MICROPROCESSOR TECHNOLOGY

Assis. Prof. Hossam El-Din Moustafa

Lecture 19

Ch.9  The Pentium II, Pentium III, and Pentium 4 Microprocessors
Chapter Objectives

- Contrast the Pentium II, III, and Pentium 4 with prior Intel microprocessors.
- Explain how the architectures of Pentium II, III, 4 improve system speed.
- Discuss the memory system of Pentium II, III, and Pentium 4 microprocessors.
The Pentium II Microprocessor

- The Pentium II is packaged on a Printed Circuit Board (PCB) instead of the integrated circuits of the past Intel microprocessors.
- Level 1 cache is 32 KB
- Level 2 cache is placed very close to the µP.
- Level 2 cache operates at ½ the µP clock frequency.
- The 400MHz Pentium II has a cache speed of 200MHz.
The Pentium II Microprocessor

- The Pentium II is available in three versions:
  1. The **full-blown** Pentium II
  2. The **Celeron**, but slot 1 circuit board does not contain level 2 cache which is located on the main board and operates at 66MHz.
  3. The **Xeon** which is the most recent version with level 2 cache of 512, 1M, 2MB. *Level 2 cache operates at the clock frequency of the µP.*
The Pentium II Microprocessor

- Early versions of Pentium II require 5V, 3.3V and variable voltage power supply for operation.
- The power supply current ranges from 8.4 to 14.2 mA depending on the operating frequency level.
- Higher power rates require good heat sink with considerable airflow.
- The heat sink and fan are built into the Pentium II cartridge. Each Pentium II output pin is capable of providing 36 mA of current.
Pin Functions

- **A20**: Address 20 Mask
- **A3→A35**: Address Buses
- **ADS**: Address Data Strobe
- **AERR**: Address error
- **AP0, AP1**: Address Parity inputs
- **BCLK**: Bus Clock sets the bus clock frequency (either 66MHz or 100MHz)
- **BERR**: Buss Error
- **BINT**: Bus Initialization
Pin Functions

- **BNR**: Bus Not Ready when equals zero, it causes the Pentium II to enter wait states.
- **BP0 to BP3**: Breakpoint pins
- **BPRI**: Bus Priority Request input
- **BR0, BR1**: Bus Request
- **BSEL**: Bus Select (not used by Pentium II)
- **D0 to D63**: Data bus connections
- **DEFER**: Indicates that the external system can not complete the bus cycle.
Pin Functions

- **DEP0→DEP7**: Data ECC (Error Check Code) pins are used in error correction scheme
- **DRDY**: Data Ready indicates that the system is presenting valid data to the Pentium II.
- **EMI**: Electro-Magnetic Interference must be grounded to prevent Pentium from generating or receiving noise.
- **FERR**: Floating-point Error
- **FLUSH**: Invalidate internal cache
Pin Functions

- **FRCERR**: Functional Redundancy check
- **HIT**: Cache contains valid data
- **HITM**: Hit Modified
- **IERR**: Internal Error
- **IGNNE**: Ignore Numeric Error
- **INIT**: Initialize Pentium II
- **INTR**: Interrupt Request
- **LINT0, LINT1**: Local APIC interrupt signals connect the appropriate pins of all APIC bus agents
Pin Functions

- **NMI**: Non-Maskable Interrupt
- **PICCLK**: Must be ¼ the frequency of BCLK
- **PICD0, PICD1**: Used for serial messages between the Pentium II and the APIC.
- **PM0, PM1**: Performance Monitor test
- **PRDY**: Probe ready output
- **PREQ**: Probe request
- **PWRGOOD**:
- **RESET**: Resets Pentium II
Pin Functions

- **REQ0 → REQ4**: Request Signals communicate commands between bus controllers and Pentium II
- **RP**: Request Parity
- **RS0 → RS2**: Request Status pins
- **RSP**: Response Parity input
- **SLP**: Sleep input (Enter sleep state)
- **SMI**: System Management Interrupt
Pin Functions

- **STPCLK**: Stop Clock
- **TCK**: Testability clock
- **TDI**: Test Data Input
- **TDO**: Test Data Output
- **TESTHI**: Test High input must be connected to +2.5V through a 1k-10K resistor for proper Pentium II operation.
Pin Functions

- **THERMTRIP**: thermal Sensor Trip output = 0 when the temperature of the Pentium II exceeds 130°C.
- **TMS**: Test Mode Select
- **TRDY**: Target ready causes Pentium II to perform a write-back operation
- **VID0→VID4**: Voltage Data output pins are either open or grounded signals that indicate what supply voltage is currently required by Pentium II
The Memory System

- The memory system is 64GB in size.
- Most systems use SDRAM operating at 66 or 100MHz.
- Pentium II memory system is divided into eight or nine banks that each store a byte of data. If the ninth byte is present, it stores an error checking code (ECC).

Fig. (9-3) Page 244 shows the memory map of a Pentium II-based computer system (IMPORTANT)
The Memory System

- The difference is the AGP area of memory
- AGP area allows the video card and Windows to access the video information in a linear address space.
- The benefit is much faster video updates because the video card does not need to page through the 128KB DOS video memory.
- Transfers between Pentium II and the memory system are controlled by the 440LX or 440BX chipset.
The Memory System

- Data transfers between Pentium II and the chipset are *eight bytes* wide.
- REQ0→REQ4 are used to communicate the chipset to the µP.

**Input/Output System:**

- The I/O port number appears on address lines A3→A15 with the bank enable signals used to select the actual memory banks used for the I/O transfer.
The Pentium III

- The Pentium III is an improved version of Pentium II.

There are two versions of Pentium III:
1. One version with 512KB cache and packaged in the slot 1 cartridge
2. The other version has 256KB cache and packaged in integrated circuit.
- The slot 1 version runs at ½ the processor speed and the integrated cache version runs at the processor clock frequency.
The Pentium III

**Chip Sets:**
- The Pentium III uses an Intel 810, 815, or 820 chipset.

**Bus:**
- The bus speed has increased to either 100MHz or 133MHz.

**Question:**
- If bus speed increases to 200 MHz, what problems would you expect? How to overcome these problems?
The Pentium 4

- The first release was in November 2000 with a speed of 1.3 GHz.
- It was available in speeds up to 2GHz

*There are two versions:*
1. The 423-pin PGA
2. The 478-pin FC-PGA2

- Both versions use 1.8 micron technology of fabrication
- Pentium 4 uses quad-pumped 100MHz memory bus speeds (Bus speed approaches 400MHz)
Memory Interface

- Memory interface to Pentium 4 uses the Intel 850 chipset
- The 850 provides a dual-pipe memory bus to the µP with each pipe interfaced to a 32-bit wide section of the memory.
- The 2 pipes function together to comprise the 64-bit wide data bus
- Memory must be populated with pairs of RDRAM memory devices operating at either 600 or 800MHz (300% increase in speed)
Register Set

- MMX registers are separate entities from the floating-point registers.
- Eight 128-bit wide XMM registers are added for use with single instruction multiple data (SIMD) instructions and the extended 128-bit packed doubled floating-point numbers.
Hyper Pipelined Technology

- The Pentium 4 has a deeper pipelined architecture than prior versions.
- Not only does it queue instructions for execution, but it also queues micro-instructions for execution in a special cache for the μP core.
- This special micro-instruction cache is 12KB
- This technology excludes the execution unit from the main cache path to the micro-instruction stream to increase performance.
Pentium 4 Mechanicals

- The power supply for the Pentium 4 is different from other ATX power supplies.
- It contains the standard ATX connector, a 12V connector, and an auxiliary connector.
- All three connectors must be plugged into the Pentium 4 main board for proper operation.
- The case for the Pentium 4 main board must have four additional standoffs to support the µP.
- The power supply should be at least 300W.
Thank You

With all best wishes !!