Chapter Objectives

- Contrast the Pentium and Pentium Pro with the 80386 and 80486 µP.
- Describe the organization of the 64-bit wide memory system.
- Detail the new instructions found in Pentium µP.
- Describe the operation of the superscalar dual integers unit and the branch prediction logic.
- Compare Pentium Pro with Pentium
- Explain the dynamic execution architecture of Pentium Pro functions.
The Pentium Pin-Out

- The Pentium µP is packaged in a 237 pin PGA.
- There are two versions: the full blown Pentium and the P24T version.
- The P24T version contains 32-bit data bus, compatible for insertion into 80486 machines.
- The P24T version comes with a fan built into the unit.
- Current versions of Pentium use a 3.3V power supply with reduced current consumptions.
Pin Functions

- **A20**: The address A20 mask input signals the Pentium to perform in Real Mode for use of the HIMEM.SYS driver.
- **A3→A31**: Address bus connections
- **ADS**: Address Data Strobe becomes active when Pentium issues a valid memory or I/O address.
- **AHold**: Address hold causes the Pentium to hold the address and AP signals for the next clock.
Pin Functions

- **AP**: Address Parity provides even parity for the memory address.
- **APCHK**: Address Parity Check = 0 when the Pentium detects an address parity error.
- **BE0→BE7**: Bank Enable signals select the access of a byte, word, double word, or quad-word of data. They are generated internally using A0→A2.
- **BOFF**: Back-Off input aborts all bus cycles.
Pin Functions

- **BP[3:2] and PM/BP[1:0]:** Breakpoint pins BP0 → BP3 indicate a breakpoint match when the debug registers are programmed to monitor for match. The Performance Monitoring pins PM0 and PM1 indicate the settings of the performance monitoring bits in the debug mode CR.

- **BRDY:** Burst Ready input signals the Pentium that the external system has applied or extracted data. It is used to insert wait states.
Pin Functions

- **BT0→BT3**: Branch Trace outputs provide bits of the branch target linear address and the default operand size on BT3.
- **BUSCHK**: Bus Check input allows the system to signal the Pentium that the bus transfer has failed.
- **CACHE**: Cache o/p indicates that the current Pentium cycle can cache data.
- **CLK**: Clock is driven by a clock signal that is at the operating frequency of the Pentium.
Pin Functions

- **D0→D63**: Data bus connections
- **D/C**: Data/Control =1 when data bus contains data for or from memory or I/O.
- **DP0→Dp7**: Data parity detects 8 memory banks
- **EADS**: External Address Strobe signals that address bus contains an address for an inquire cycle.
- **EWBE**: External Write Buffer Empty input indicates that the write cycle is pending.
Pin Functions

- **FERR**: Floating Point Error shows that the internal coprocessor has erred.
- **FLUSH**: Flush cache input causes the cache to flush all write-back lines and invalidate its internal caches.
- **FRCMC**: Functional Redundancy Check configure the Pentium in the master mode (1) or checker mode (0).
- **HIT**: Hit shows that the internal cache contains valid data in the inquire mode.
**Pin Functions**

- **HITM:** Hit Modified shows that the inquire cycle found a modified cache line.
- **HOLD:** Hold requests DMA action
- **HLDA:** Hold Acknowledge
- **IBT:** Instruction Branch Taken indicates that the µP has taken an instruction branch.
- **IERR:** Internal Error o/p shows that the Pentium has detected an internal parity error.
- **IGNNE:** Ignore Numeric Error
Pin Functions

- **INIT**: Initialization input performs a reset without initializing the cache, write back buffers, and floating point registers.
- **INTR**: Interrupt Request
- **INV**: Invalidation input determines the cache line state after an inquiry.
- **IU**: U-Pipe instruction complete o/p shows that the instruction in the U-Pipe is complete.
- **IV**: V-Pipe instruction complete o/p shows that the instruction in the V-Pipe is complete.
Pin Functions

- **KEN**: Cache Enable input enables internal caching.
- **LOCK**: Lock pin
- **M/IO**: Memory/Input-Output
- **NA**: Next Address indicates that the external memory system is ready to accept a new bus cycle.
- **NMI**: Non-Maskable Interrupt
- **PCD**: Page Cache disable reflects the state of the PCD bit in CR3.
Pin Functions

- **PCHK**: Parity Check o/p indicates a parity check error for data read.
- **PEN**: Parity Enable i/p enables the machine check interrupt.
- **PRDY**: Probe Ready o/p indicates that the probe mode has been entered for debugging.
- **PWT**: Page Write Through o/p shows the state of the PWT bit in CR3.
- **R/S**: A pin which is used with Intel Debugging Port and causes an interrupt.
Pin Functions

- **RESET**: Initializes the Pentium
- **SCYC**: Split Cycle o/p signals a misaligned locked bus cycle.
- **SMI**: System Management Interrupt i/p causes the Pentium to enter the system management mode of operation.
- **SMIACT**: System Management Interrupt Active o/p shows that the Pentium is operating in the system management mode.
Pin Functions

- **TCK**: Testability Clock i/p selects the clocking function.
- **TDI**: Test Data i/p is used to test data clocked into the Pentium with the TCK signal.
- **TDO**: Test Data o/p is used to gather test data and instructions shifted out with TCK.
- **TMS**: Test Mode Select i/p controls the operation of the Pentium in test mode.
- **TRST**: Test Reset i/p allows the test mode to be reset.
Pin Functions

- **W/R:** Write/Read
- **WB/WT:** Write-Back/Write-Through selects the operation for the Pentium data cache.
The Memory System

- The memory system is 4GB
- The Pentium uses 64-bit data bus to address memory organized in 8 banks, each contains 512MB of data. (Fig. 8.2 P. 213)
- The 64-bit wide memory is important to read double-precision floating point data in one read cycle instead of two in the 80486.
- Memory selection is accomplished with the bank enable signals BE0 → BE7.
The Memory System

- Pentium can check and generate parity for the address bus during certain operations through the pin **AP**.

**Question:**
*How is a 32-bit memory system connected to Pentium?*

**Answer:**
- By using a multiplexer to convert the 64-bit data bus to a 32-bit data bus.
- **Note:** All double-words must be stored at double-word **boundaries** (addresses divisible by 4).
System Timing

- The basic Pentium non-pipelined memory cycle consists of two clocking periods T1 and T2.
- During T1, the µP issues the ADS, W/R, and M/IO signals.
- During T2, the data bus is sampled in synchronization with the end of T2 at the positive transition of the clock pulse.
- Wait states are inserted into the timing by controlling the BRDY input to the Pentium.
- *The burst cycle in Pentium transfers four 64-bit numbers in 5 clocking periods.*
Branch Prediction Logic

- Pentium uses a branch prediction logic to reduce the time required for a branch caused by internal delays.
- When a branch instruction is encountered, the µP begins pre-fetch instruction at the branch address.
- Instructions are loaded into the instruction cache, so when a branch occurs, the instructions are present and allow the branch to execute in one clocking period instead of four.
Cache Structure

- The Pentium contains two 8KB cache memories instead of one.
- There is an 8KB data cache and an 8KB instruction cache.

Superscalar Architecture:
- The Pentium is organized with 3 execution units (3 instructions can be executed simultaneously)
- One executes floating point instructions.
- The other two (U-Pipe and V-Pipe) execute integer instructions.
Control Registers

- **CR4** is new with the following new bits:
- **CD**: Cache Disable, if CD=1, the cache will not fill with new data for cache misses.
- **NW**: Not-Write Through selects the mode of operation for the data cache.
- **AM**: Alignment Mask enables alignment checking when set.
- **WP**: Write Protect, protects user level pages against supervisor level write operations.
Control Registers

- **NE**: Numeric Error enables standard numeric coprocessor error detection.
- **VME**: Virtual Mode Extension, enables support for the virtual interrupt flag in protected mode.
- **PVI**: Protected mode Virtual Interrupt enables support for the virtual interrupt flag in protected mode.
- **TSD**: Time Stamp Disable controls the RDTSC instruction.
Control Registers

- **DE**: Debugging Extension, enables I/O breakpoint extensions when set.
- **PSE**: Page Size Extension enables 4MB memory pages when set.
- **MCE**: Machine Check Enable, enables machine checking interrupt.
EFLAGS Register

- Four new flag bits have been added:
  - **ID**: Identification flag is used to test for the CPUID instruction.
  - **VIP**: Virtual Interrupt Pending
  - **VIF**: Virtual Interrupt Flag
  - **AC**: Alignment Check indicates the state of the AM bit in CR0
Built-In-Self-Test (BIST)

- The BIST is accessed on power up by placing a logic 1 on INIT while the RESET pin changes from 1 to 0.
- The BIST tests 70% of the internal structure of the Pentium in 150 µs.
- The outcome is reported in register EAX.
- If EAX=0, the BIST passed and the Pentium is ready for operation.
- If EAX contains other value, the Pentium has malfunctioned and is faulty.
Thank You

With all best wishes !!